CMOS 80 MHz Monolithic 256 × 24(18) Color Palette RAM-DACs

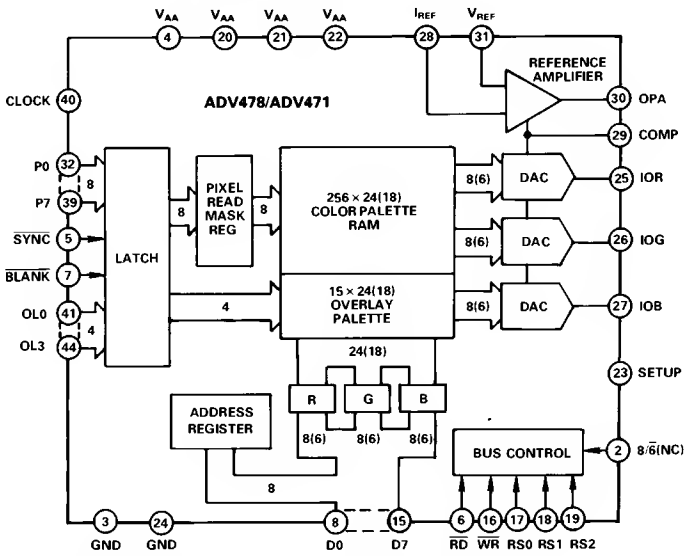
ADV478/ADV471

FEATURES
Personal System/2* Compatible
80 MHz Pipelined Operation
Triple 8-Bit (6-Bit) D/A Converters
256 × 24(18) Color Palette RAM
15 × 24(18) Overlay Registers
RS-343A/RS-170 Compatible Outputs
Sync on All Three Channels
Programmable Pedestal (0 or 7.5 IRE)
External Voltage or Current Reference
Standard MPU Interface
+5 V CMOS Monolithic Construction
44-Pin PLCC Package
Power Dissipation: 800 mW

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES
80 MHz
66 MHz
50 MHz
35 MHz

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. NUMBERS IN PARENTHESIS INDICATE PIN NAMES FOR THE ADV471.
2. NC = NO CONNECT

GENERAL DESCRIPTION

The ADV478 (ADV®) and ADV471 are pin compatible and software compatible RAM-DACs designed specifically for Personal System/2 compatible color graphics.

The ADV478 has a 256 × 24 color lookup table with triple 8-bit video D/A converters. It may be configured for either 6 bits or 8 bits per color operation. The ADV471 has a 256 × 18 color lookup table with triple 6-bit video D/A converters.

Options on both parts include a programmable pedestal (0 or 7.5 IRE) and use of an external voltage or current reference.

Fifteen overlay registers provide for overlaying cursors, grids, menus, EGA emulation, etc. Also supported is a pixel read mask register and sync generation on all three channels.

The ADV478 and ADV471 generate RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering. Differential and integral linearity errors are guaranteed to be a maximum of ±1 LSB for the ADV478 and ±1/4 LSB for the ADV471 over the full temperature range.

REV. B

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ADV478/ADV471–SPECIFICATIONS

(V_{AA}[1] = +5 V, SETUP = 8/$\overline{6}$ = V_{AA}, V_{REF} = +1.235 V. R_{SET} = 147 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)[3]	8 (6)	Bits	
Accuracy (Each DAC)[3]			
Integral Nonlinearity	±1 (1/4)	LSB max	
Differential Nonlinearity	±1 (1/4)	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	
Coding	Binary		
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4 V or 2 .4 V
Input Capacitance, C_{IN}	7	pF max	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	50	μA max	
Floating-State Output Capacitance	7	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	20	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05 mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
(SETUP = V_{AA})	1.90	mA max	
Black Level Relative to Blank	0	μA min	Typically 5 μA
(SETUP = GND)	50	μA max	
Blank Level	6.29	mA min	Typically 7.62 mA
	8.96	mA max	
Sync Level	0	μA min	Typically 5 μA
	50	μA max	
LSB Size[3]	69.1 (279.68)	μA typ	8/$\overline{6}$ = Logical 1 for ADV478
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	–1	V min	
	+1.5	V max	
Output Impedance, R_{OUT}	10	kΩ typ	
Output Capacitance, C_{OUT}	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	
Input Current, I_{VREF}	10	μA typ	Tested in Voltage Reference Configuration with V_{REF} = 1.235 V
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	80 MHz and 66 MHz Parts
	4.50/5.50	V min/V max	50 MHz and 35 MHz Parts
Supply Current, I_{AA}	220	mA max	Typically 180 mA
Power Supply Rejection Ratio	0.5	%/% max	f = 1 kHz, COMP = 0.1 μF
Power Dissipation	1100	mW max	Typically 900 mW, V_{AA} = 5 V
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[4, 5]	–30	dB typ	
Glitch Impulse[4, 5]	75	pV secs typ	
DAC to DAC Crosstalk[6]	–23	dB typ	

NOTES

[1]±5% for 80 MHz and 66 MHz parts; ±10% for 50 MHz and 35 MHz parts.

[2]Temperature Range (T_{MIN} to T_{MAX}); 0°C to +70°C.

[3]Numbers in parentheses indicate ADV471 parameter value.

[4]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2 × clock rate.

[5]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, D0–D7 output load ≤50 pF. See timing notes in Figure 2.

[6]DAC to DAC crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA}[2] = +5 V, SETUP = 8/$\overline{6}$ = V_{AA}, V_{REF} = 1.235 V. R_{SET} = 147 Ω. All Specifications T_{MIN} to T_{MAX}[3].)

Parameter	KP80 Version	KP66 Version	KP50 Version	KP35 Version	Units	Conditions/Comments
f_{MAX}	80	66	50	35	MHz	Clock Rate
t_1	10	10	10	10	ns min	RS0–RS2 Setup Time
t_2	10	10	10	10	ns min	RS0–RS2 Hold Time
t_3	5	5	5	5	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4	40	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5	20	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6	10	10	10	10	ns min	Write Data Setup Time
t_7	10	10	10	10	ns min	Write Data Hold Time
t_8	50	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_9	$6 \times t_{12}$	$6 \times t_{12}$	$6 \times t_{12}$	$6 \times t_{12}$	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{10}	3	3	3	3	ns min	Pixel and Control Setup Time
t_{11}	3	3	3	3	ns min	Pixel and Control Hold Time
t_{12}	12.5	15.3	20	28	ns min	Clock Cycle Time
t_{13}	4	5	6	7	ns min	Clock Pulse Width High Time
t_{14}	4	5	6	9	ns min	Clock Pulse Width Low Time
t_{15}	30	30	30	30	ns max	Analog Output Delay
t_{16}	3	3	3	3	ns typ	Analog Output Rise/Fall Time
t_{17}[4]	13	15.3	20	28	ns typ	Analog Output Settling Time
t_{18}	2	2	2	2	ns max	Analog Output Skew
t_{PD}	$4 \times t_{12}$	$4 \times t_{12}$	$4 \times t_{12}$	$4 \times t_{12}$	ns min	Pipeline Delay

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, 37.5 Ω. D0–D7 output load ≤50 pF. See timing notes in Figure 2.
[2]±5% for 80 MHz and 66 MHz parts; ±5% for 50 MHz and 35 MHz parts.
[3]Temperature Range (T_{MIN} to T_{MAX}); 0°C to +70°C.
[4]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic.

Specifications subject to change without notice

TIMING DIAGRAMS

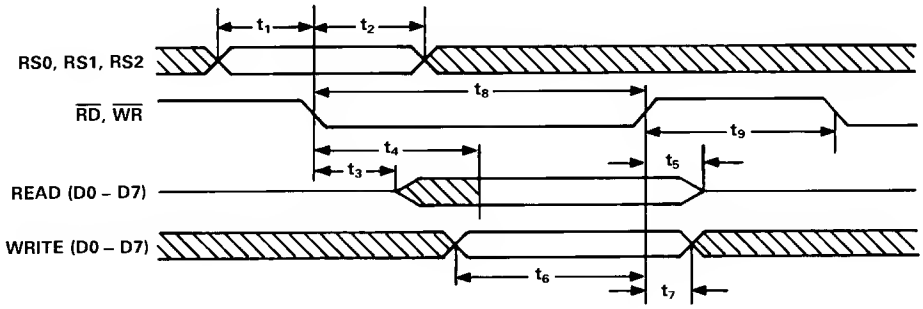
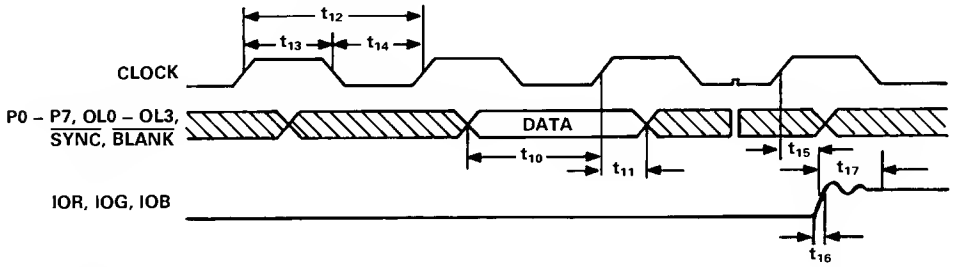


Figure 1. MPU Read/Write Timing



NOTES
1. OUTPUT DELAY (t_{15}) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL SCALE TRANSITION.
2. SETTLING TIME (t_{17}) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1LSB (ADV478) OR ±1/4LSB (ADV471).
3. OUTPUT RISE/FALL TIME (t_{16}) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

Figure 2. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}				
80 MHz, 66 MHz Parts		4.75	5.00	5.25	Volts
50 MHz, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts
Current Reference Configuration					
Reference Current	I_{REF}	–3		–10	mA

CAUTION

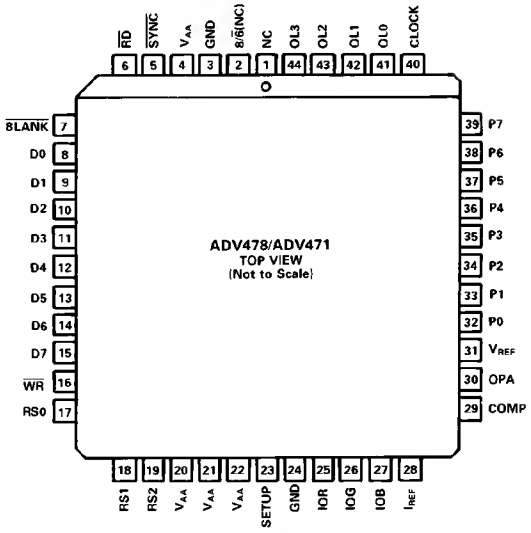
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV478/ADV471 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND ..... +7 V
Voltage on Any Digital Pin .... GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) ..... –55°C to +125°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Junction Temperature (T_J) ..... +150°C
Vapor Phase Soldering (1 minute) ..... 220°C
IOR, IOB, IOG to GND[2] ..... 0 V to V_{AA}

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

PLCC PIN CONFIGURATION



NOTES
1. NUMBERS IN PARENTHESIS INDICATE PIN NAMES FOR THE ADV471.
2. NC=NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Color Palette RAM	Speed	Package Option*
ADV471KP80	0°C to +70°C	256 × 18	80 MHz	P-44A
ADV471KP66	0°C to +70°C	256 × 18	66 MHz	P-44A
ADV471KP50	0°C to +70°C	256 × 18	50 MHz	P-44A
ADV471KP35	0°C to +70°C	256 × 18	35 MHz	P-44A
ADV478KP80	0°C to +70°C	256 × 24	80 MHz	P-44A
ADV478KP66	0°C to +70°C	256 × 24	66 MHz	P-44A
ADV478KP50	0°C to +70°C	256 × 24	50 MHz	P-44A
ADV478KP35	0°C to +70°C	256 × 24	35 MHz	P-44A

*P = Plastic Leaded Chip Carrier (PLCC).

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level as illustrated in Tables IV and V. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logical zero, the pixel and overlay inputs are ignored
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 3 and 4). $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Tables IV and V; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table III. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figures 5 and 6).
I_{REF}	Full-scale adjust control. Note that the IRE relationships in Figures 3 and 4 are maintained, regardless of the full-scale output current. When using an external voltage reference (Figure 5), a resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between R_{SET} and the full-scale output current on each output is: $R_{SET}\ (\Omega) = K \times 1{,}000 \times V_{REF}\ (V)/I_{OUT}\ (mA)$ K is defined in the table below, along with corresponding R_{SET} values for doubly terminated 75 Ω loads. When using an external current reference (Figure 6), the relationship between I_{REF} and the full-scale output current on each output is: $I_{REF}\ (mA) = I_{OUT}\ (mA)/K$
COMP	Compensation pin. If an external voltage reference is used (Figure 5), this pin should be connected to OPA. If an external current reference is used, this pin should be connected to I_{REF}. A 0.1 μF ceramic capacitor must always be used to bypass this pin to V_{AA}.
V_{REF}	Voltage reference input. If an external voltage reference is used (Figure 5), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 6), this pin should be left floating, except for the bypass capacitor. A 0.1 μF ceramic capacitor must always be used to decouple this input to V_{AA} as shown in Figures 5 and 6.
OPA	Reference amplifier output. If an external voltage reference is used (Figure 5), this pin must be connected to COMP. When using an external current reference (Figure 6), this pin should be left floating.
V_{AA}	Analog power. All V_{AA} pins must be connected to the Analog Power Plane.
GND	Analog ground. All GND pins must be connected to the Ground Plane.
$\overline{\text{WR}}$	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of $\overline{\text{WR}}$, and RS0–RS2 are latched on the falling edge of $\overline{\text{WR}}$ during MPU write operations. See Figure 1.

Mode	Pedestal	K	R_{SET} (Ω)
6-Bit	7.5 IRE	3.170	147
8-Bit	7.5 IRE	3.195	147
6-Bit	0 IRE	3.000	147
8-Bit	0 IRE	3.025	147

PIN FUNCTION DESCRIPTION (Continued)

Pin Mnemonic	Function
$\overline{RD}$	Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS0–RS2 are latched on the falling edge of $\overline{RD}$ during MPU read operations.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed as illustrated in Tables I and II.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
8/$\overline{6}$	8-bit/6-bit select input (TTL compatible). This control input specifies whether the MPU is reading and writing 8-bits (logical one) or 6-bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and are logical zero during color read cycles). This control input is implemented only on the ADV478.

TERMINOLOGY

Blanking Level
The level separating the SYNC portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs would be required, one for each color.

Composite SYNC Signal (SYNC)
The portion of the composite video signal which synchronizes the scanning process.

Composite Video Signal
The video signal with or without setup, plus the composite SYNC signal.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Setups
The difference between the reference black level and the blanking level.

SYNC Level
The peak level of the composite SYNC signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

CIRCUIT DESCRIPTION

MPU Interface

As illustrated in the functional block diagram, the ADV478 and ADV471 support a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers or read mask register, as shown in Table I. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers.

To write color data, the MPU writes to the address register (selecting RAM or overlay write mode) with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green and blue), using RS0–RS2 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the ADV471) and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green and blue data.

Table I. Control Input Truth Table

RS2	RS1	RS0	Addressed by MPU
0	0	0	Address Register (RAM Write Mode)
0	1	1	Address Register (RAM Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register
1	0	0	Address Register (Overlay Write Mode)
1	1	1	Address Register (Overlay Read Mode)
1	0	I	Overlay Registers
1	1	0	Reserved

To read color data, the MPU loads the address register (selecting RAM or overlay read mode) with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (8 or 6 bits each of red, green and blue), using RS0–RS2 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green and blue data.

When accessing the color palette RAM, the address register resets to 00H following a blue read or write cycle to RAM location FFH. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the four most significant bits of the address register (ADDR4-7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G and B in the block diagram) are synchronized by internal logic and occur in the period between MPU accesses. As only one pixel clock cycle is required to complete the transfer, the color palette RAM and overlay registers may be accessed at any time with no noticeable disturbance on the display screen.

To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle (ADDR0–7), are accessible to the MPU and are used to address color palette RAM locations and overlay registers, as shown in Table II. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing.

Table II. Address Register (ADDR) Operation

	Value	RS2	RS1	RS0	Addressed By MPU
ADDRa,b (Counts Modulo 3)	00				Red Value
	01				Green Value
	10				Blue Value
ADDR0–7 (Counts Binary)	00H–FFH	0	0	1	Color Palette RAM
	XXXX 0000	1	0	1	Reserved
	XXXX 0001	1	0	1	Overlay Color 1
	XXXX 0010	1	0	1	Overlay Color 2
	•	•	•	•	•
	•	•	•	•	•
	XXXX 1111	1	0	1	Overlay Color 15

ADV478 Data Bus Interface

On the ADV478, the 8/$\overline{6}$ control input is used to specify whether the MPU is reading and writing 8 bits (8/$\overline{6}$ = logical one) or 6 bits (8/$\overline{6}$ = logical zero) of color information each cycle.

For 8-bit operation, Do is the LSB and D7 is the MSB of color data.

For 6-bit operation (and also when using the ADV471), color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

ADV471 Data Bus Interface

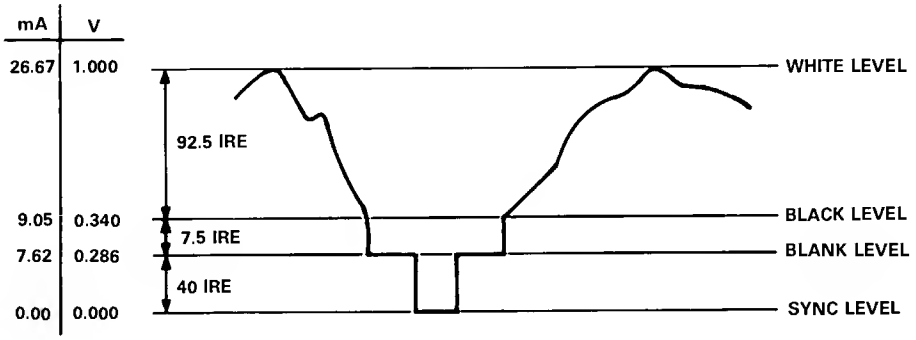
Color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table III.

Table III. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = FFH)

OL0-OL3	P0-P7	Addressed by Frame Buffer
0H	00H	Color Palette RAM Location 00H
0H	01H	Color Palette RAM Location 01H
•	•	•
•	•	•
0H	FFH	Color Palette RAM Location FFH
1H	XXH	Overlay Color 1
2H	XXH	Overlay Color 2
•	•	•
•	•	•
FH	XXH	Overlay Color 15



NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = V_{AA}.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 3. Composite Video Output Waveform (SETUP = V_{AA})

Table IV. Video Output Truth Table (SETUP = V_{AA})

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE LEVEL	26.67	1	1	FFH
DATA	data + 9.05	1	1	data
DATA-SYNC	data + 1.44	0	1	data
BLACK LEVEL	9.05	1	1	00H
BLACK-SYNC	1.44	0	1	00H
BLANK LEVEL	7.62	1	0	xxH
SYNC LEVEL	0	0	0	xxH

NOTES
[1]Typical with full-scale IOG = 26.67 mA, SETUP = V_{AA}.
External voltage or current reference adjusted for 26.67 mA full-scale output.

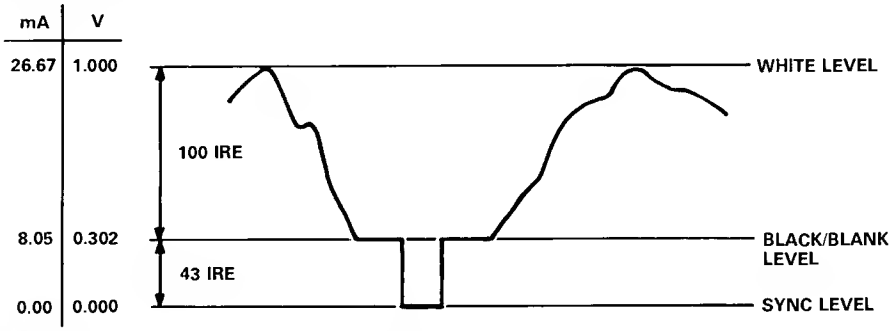
The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits for the ADV471) of color information to the three D/A converters.

For additional information on Pixel Mask Register, see application note "Animation Using the Pixel Read Mask Register of the ADV47X Series of Video RAM-DACs" (Publication Number E1316–15–10/89).

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Tables IV and V detail how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal is to be used.

The analog outputs of the ADV478 and ADV471 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.



NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = GND.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 4. Composite Video Output Waveform (SETUP = GND)

Table V. Video Output Truth Table (SETUP = GND)

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE LEVEL	26.67	1	1	FFH
DATA	data+8.05	1	1	data
DATA-SYNC	data	0	1	data
BLACK LEVEL	8.05	1	1	00H
BLACK-SYNC	0	0	1	00H
BLANK LEVEL	8.05	1	0	xxH
SYNC LEVEL	0	0	0	xxH

NOTE
[1]Typical with full-scale IOG = 26.67 mA, SETUP = GND.
External voltage or current reference adjusted for 26.67 mA full-scale output.

PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

The layout should be optimized for lowest noise on the ADV478/ADV471 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV478/ADV471 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the ADV478/ADV471, the analog output traces and all the digital signal traces leading up to the ADV478/ADV471.

Power Planes

The ADV478/ADV471 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figures 5 and 6. This bead should be located within three inches of the ADV478/ADV471.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV478/ADV471 power pins and current/voltage reference circuitry.

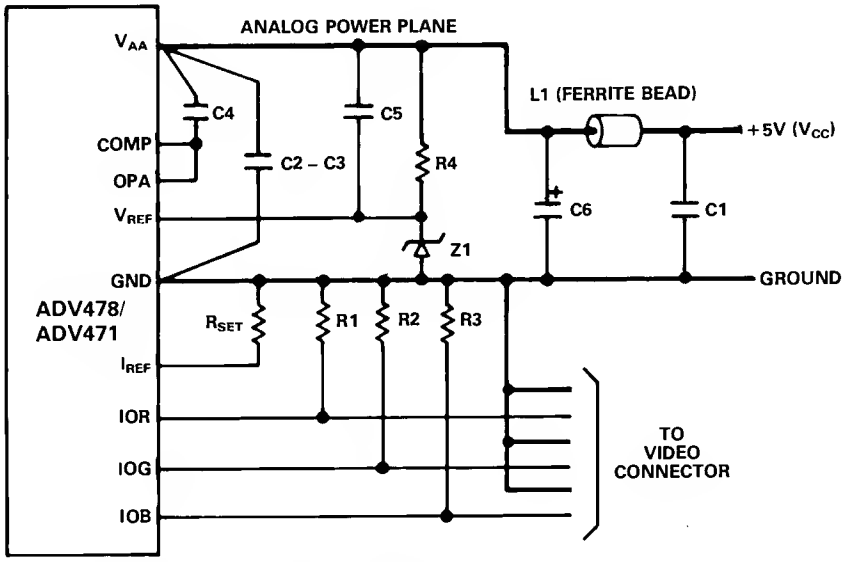
Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Best performance is obtained with a 0.1 μF ceramic capacitor decoupling each of the two groups of V_{AA} pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV478 and ADV471 contain circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1μF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10μF Tantalum Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75Ω 1% Metal Film Resistor	Dale CMF-55C
R4	1kΩ 5% Resistor	
R_{SET}	1% Metal Film Resistor	Dale CMF-55C
Z1	1.2V Voltage Reference	Analog Devices AD589KH

Figure 5. Typical Connection Diagram and Component List (External Voltage Reference)

Digital Signal Interconnect

The digital inputs to the ADV478/ADV471 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV478/ADV471 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

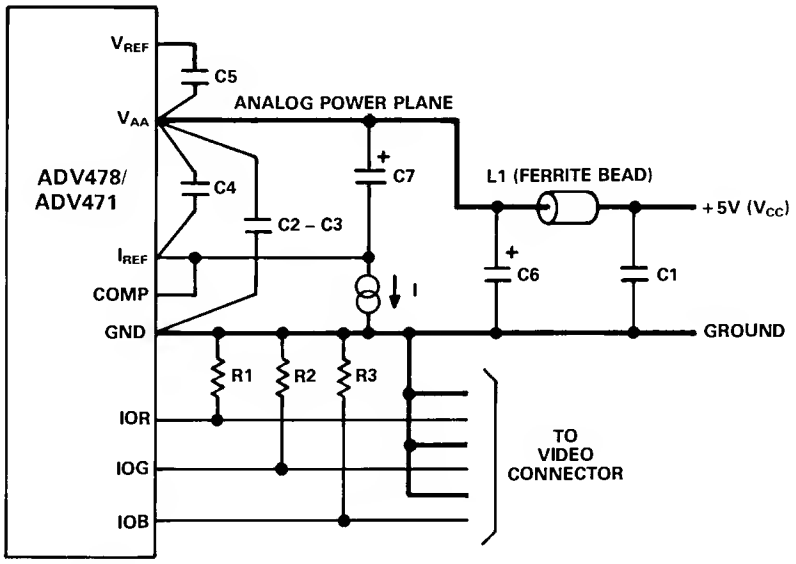
Analog Signal Interconnect

The ADV478/ADV471 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75 Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the ADV478/ADV471 to minimize reflections.

NOTE: Additional information on PC Board layout can be obtained in an application note entitled "Design and Layout of a Video Graphics System for Reduced EMI" from Analog Devices (Publication Note E1309–15–10/89).



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1μF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10μF Tantalum Capacitor	Mallory CSR13G106KM
C7	47μF Tantalum Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75Ω 1% Metal Film Resistor	Dale CMF-55C

Figure 6. Typical Connection Diagram and Component List (External Current Reference)

APPLICATION INFORMATION

EXTERNAL VOLTAGE VS. CURRENT REFERENCE

The ADV478/ADV471 is designed to have excellent performance using either an external voltage or current reference. The voltage reference design (Figure 5) has the advantages of temperature compensation, simplicity, lower cost and provides excellent power supply rejection. The current reference design (Figure 6) requires more components to provide adequate power supply rejection and temperature compensation (two transistors, three resistors and additional capacitors).

RS-170 Video Generation

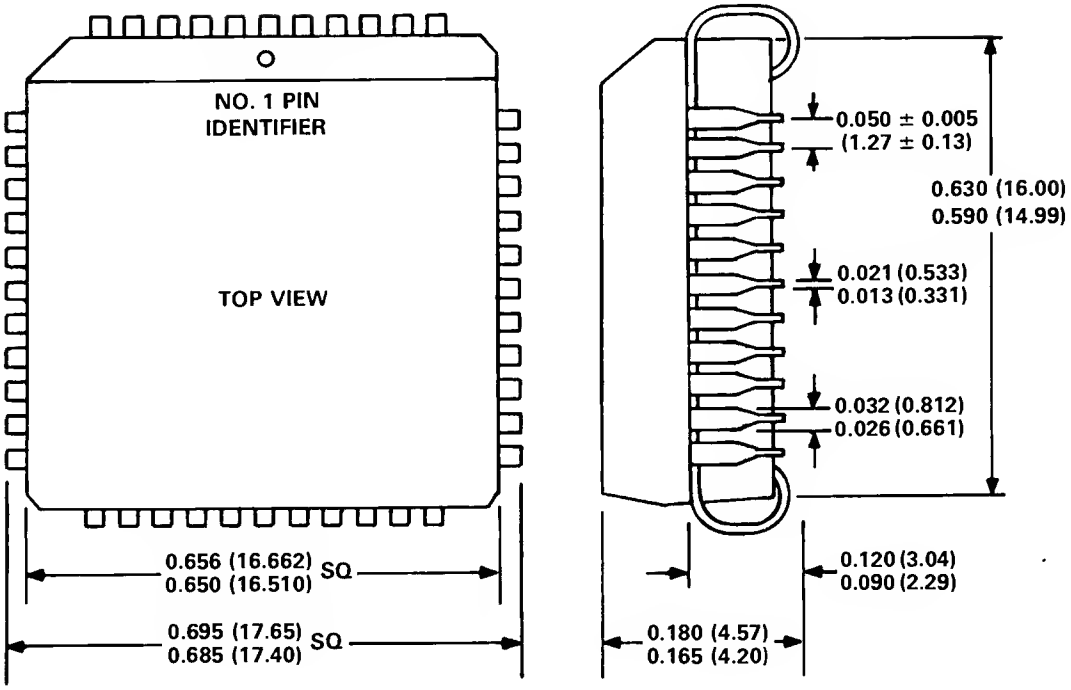
For generation of RS-170 compatible video, it is recommended that the DAC outputs be connected to a singly terminated 75 Ω load. If the ADV478/ADV471 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75 Ω and singly terminated 75 Ω loads.

If driving a large capacitive load (load $RC > 1/(2\pi f_C)$), it is recommended that an output buffer (such as an AD848 or AD9617 with an unloaded gain>2) be used to drive a doubly terminated 75 Ω load.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Terminal Plastic Leaded Chip Carrier
P-44A



C1197–24–6/88

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